SYSTRON DONNER

A THORN EMI company

SYSTRON DONNER
Member THORN EMI Group

MODEL 218
DATA/PULSE GENERATOR
SERIAL NO.
(B)

INSTRUMENT DIVISION

OPERATING AND SERVICE MANUAL

2727 Systron Drive • Concord, California 94518 • U.S.A.
Tel: (415) 676-5000 • TWX: 910-481-9479 • Cable: SYSTRON DONNER
FSCM No. 52542

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SYSTRON DONNER
INSTRUMENT DIVISION
2727 Systron Drive
Concord, California 94518

WARRANTY POLICY

I Warranty

Systron Donner Instrument Division warrants that at the time of shipment the products manufactured by Systron Donner and sold hereunder will be free from defects in material and workmanship and will conform to the current specifications published by Systron Donner's Instrument Division.

II Warranty

A The warranty period will be one year from the date of shipment. This warranty is extended only to the original buyer.

III Warranty Adjustments

A. If any defect within this warranty appears, Purchaser shall notify Seller immediately.

B Systron Donner agrees to repair or furnish a replacement for, but not install, any product which within the standard warranty shall, upon test and examination by Systron Donner, prove defective within the above warranty period.

C No product will be accepted for return or replacement without prior approval of Systron Donner. Upon such authorization and in accordance with instructions of Systron Donner, the product will be returned to the manufacturing location, shipping charges prepaid by Purchaser.

IV Exclusions from Warranty

A The foregoing warranty is in lieu of and excludes all other expressed or implied warranties of merchantability or fitness or otherwise.

B Systron Donner will not be liable for any special or consequential damages or for loss, damages or expense directly or indirectly arising from the use of the products, or any inability to use them either separately or in combination with any other equipment or material, or from any other cause.

C The warranty does not extend to any product manufactured by Systron Donner which has been subjected to misuse, neglect, accident, improper installation or to use in violation of instructions furnished by Systron Donner.

D The warranty does not extend to or apply to any unit which has been repaired or altered at any place other than Systron Donner; by persons not expressly approved by Systron Donner; not to any unit, the serial number of which has been removed or defaced or Changed.

E This warranty applies to new equipment only and will cover repaired or replacement items only to the extent of the balance remaining of the items original warranty period noted in Paragraph II.

F All freight charges will be paid for by the Purchaser.

June, 1985

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INSTRUMENT
DIVISION

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Phone (415) 676-5000
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LIST OF DRAWINGS

41000-261 Block Diagram - Model 218
40000-497 Schematic, Clock Generating Circuits
40000-498 Schematic, Logic Circuit
40000-499 Schematic, Output Amplifier
40000-500 Schematic, Power Supply ±15 V, +5 V

CHAPTER 1

GENERAL DESCRIPTION

1) INTRODUCTION

The Model 218 combines the capabilities of a high-speed pulse generator and the versatility of a 16-bit data generator to offer a low cost instrument of unlimited capability. Operated as a data generator, the Model 218 produces 16-bit words in either NRZ or RZ format with data content controlled by front panel pushbuttons. A remote programming option is available. Words may be recycled continuously, manually or by external command, either synchronously or asynchronously. Two or more Model 218's may be operated in parallel for multi-channel outputs or in series for longer word lengths. Operated as a pulse generator (or in the RZ data mode), pulse width is continuously variable from 10 ns to 100 ms in seven ranges.

TABLE 1.1 SPECIFICATIONS

Repetition Rate	Continuously variable from 10 Hz to 50 MHz in seven ranges.
Sync Gate	In the pulse format or the continuous recycle mode the instrument can be sync gated by a +2 V signal. The first clock pulse occurs approximately 20 ns after the gate signal. (This provides the capability of varying the word lengths.)
External Trigger	The instrument may be triggered by an external source with +2 V peak amplitude signal at rep rates from 0 to 50 MHz.
Manual Trigger	Data cycle (16-bit word) advances one bit each time the MANual pushbutton is depressed.
Data Cycle	Fixed at 16 bits. DATA CONTENT pushbuttons determine the state (true or false) of each bit. Two or more instruments may be operated in parallel to form a multiple channel system, or in series to form longer word lengths without pattern limitations.
Recycle Modes:	
Continuous	Serial words repeated sequentially without interruption.
Async Command	A 16-bit word is generated for each command signal (+2 V pulse). The clock is not synchronized with the recycle command.

TABLE 1.1 SPECIFICATIONS (Cont'd)

Recycle Modes (Cont'd):	
Sync Command	A 16-bit word is generated for each command signal (+2 V pulse). The clock is synchronized with the recycle command. The clock sync output is a burst of pulses after each recycle command.
Manual	A 16-bit word is generated each time the MANual pushbutton is depressed.
Data Format:	NRZ, RZ or PULSE, selectable by a front panel switch.
NRZ	Each data bit remains in the same state (true or false) for the entire clock period.
RZ	The portion of the clock period in which a bit remains in the true state is determined by the width controls. Maximum RZ width duty cycle is 70% of clock period at rep rates from 10 Hz to 10 MHz, decreasing to 50% of clock period from 10 MHz to 50 MHz.
Pulse	In the pulse mode, the instrument functions as a pulse generator. Pulse width is variable by means of the width controls. The digital portion of the instrument is disabled in this mode.
Pulse Width	In the pulse or RZ data mode, the width is continuously variable from 10 ns to 100 ms in seven ranges. Maximum duty cycle is 70% of clock period at rep rates from 0 to 10 MHz, decreasing to 50% at rep rates from 10 to 50 MHz.
Bit 16 Selectable RZ or NRZ	In the recycle command modes and for NRZ format, bit 16 may be selected to be either true NRZ (remain true or false until bit 1 of the next recycle occurs) or may be returned to zero one clock period after bit 16 begins.
Data Outputs	Simultaneous positive true and complement outputs are provided from 50 ohm sources. Rise/fall times are approximately 5 ns when terminated with 50 ohms.
Output Levels (into 50 ohms)	Upper level is continuously variable from -4 V to +5 V (-8 V to +10 V open circuit). Lower level is continuously variable from -5 V to +4 V (-10 V to +8 V open circuit). Maximum difference between levels is 5 V (10 V open circuit).

TABLE 1.1 SPECIFICATIONS (Cont'd)

Sync Outputs	
Clock Sync	Occurs at the data rate.
Bit 1 Sync	Occurs approximately 20 ns before the first bit in each data cycle (16-bit word).
Bit 16 Sync	Occurs approximately 40 ns before the last bit in each data cycle (16-bit word).
Output Protection	Short circuits to ground, voltages up to ±10 V or any combination of control settings will not damage the output.
Operating Temperature	0° to 50°C.
Power Required	Approximately 50 W, 50-400 Hz at 105-125/210-250 V ac, selectable by means of a multitap transformer and a range switch located on the back panel.
Physical Characteristics	Front panel is brushed aluminum finish with black markings. Input and output connectors are BNC type.
Dimensions	16-3/4" W x 3½" H x 14-5/8" D.
Shipping Weight	Approximately 17 pounds. The instrument may be rack mounted by installing a Type 1010 Rack Mounting Set.
Accessories Furnished	One 8-foot, 3-prong conductor power cord and one maintenance handbook.
Accessories Available	Type 1010 Rack Mounting Set, 2003A Power Termination, 2101 Inverting Transformer (for sync outputs only), 2302 Pulse Mixer, 2401 Rise Time Integrator and extra handbooks.
Remote Programming Option	Logic Levels
Logic Levels	Zero volts inhibits, +2 V enables.
Programming Time	<50 ns per bit.
Programming Lines	16 lines (one for each bit) and one line for ground return.
Programming Connector	Winchester 18 pin female, Type XMRE rear mount.
Accessories Furnished	Mating program connector.

CHAPTER 2
CONTROLS AND CONNECTORS

2.1 POWER Switch	Applies ac voltage to the transformer primary and illuminates the power lamp.
2.2 CLOCK RATE Controls	The pushbuttons select either MANual, EXT or one of seven available ranges the vernier provides continuous control within the range selected. When the EXT pushbutton is depressed, the instrument can be triggered by an external source at repetition rates from 0 to 50 MHz. When the MAN pushbutton is depressed, manual triggered is selected and each time it is depressed thereafter the data output advances one (1) bit period.
2.3 WIDTH Controls	The pushbuttons select one of seven available ranges and the vernier provides continuous control of the pulse width within the range selected when the instrument is in the RZ or PULSE.
2.4 DATA CONTENT Pushbuttons	Determines the state of each bit in the data output. The bit is true when the pushbutton is depressed and false when the pushbutton is released.
2.5 FORMAT Pushbuttons	Select output format to be either NRZ, RZ or PULSE.
2.5.1 NRZ	When NRZ pushbutton is depressed each true bit in the data output remains true for the entire bit period.
2.5.2 RZ	When the RZ pushbutton is depressed, each true bit in the data output remains true for the period of time determined by the WIDTH controls.
2.5.3 PULSE	When the PULSE pushbutton is depressed, the instrument functions as a pulse generator.
2.6 RECYCLE Pushbuttons	
2.6.1 CONT	In this mode 16-bit words are repeated sequentially without interruption.
2.6.2 COMMAND	
2.6.2.1 SYNC	In the SYNC COMMAND mode, a 16-bit word is generated for each command signal (+2 V pulse) at the recycle input. The clock is synchronized with the recycle command signal resulting in synchronous data.

2.6.2.2 ASYNC	In the ASYNC COMMAND mode, a 16-bit word is generated for each command signal (+2 V pulse) at the RECYCLE input. The clock is not synchronized with the recycle command signal, resulting in asynchronous data.
2.6.2.3 MAN	A 16-bit word is generated each time the MAN RECYCLE COMMAND pushbutton is depressed.
2.7 SYNC GATE Switch	In the ON position, the output can be gated by a signal (+2 V pulse) at the SYNC GATE input when the instrument is in the pulse format or the continuous recycle mode.
2.8 BIT 16 Switch	In the recycle command modes and for NRZ format, Bit 16 may be selected to be either NRZ or RZ.
2.8.1 NRZ Position	Bit 16 remains true or false until Bit 1 of the next recycle occurs.
2.8.2 RZ Position	Bit 16 returns to zero one clock period after Bit 16 begins
2.9 OUTPUT LEVELS Controls	The maximum difference between the upper and lower levels of the data output is limited to 5 V when the output is terminated with 50 ohms (10 V open circuit).
2.9.1 UPPER LEVEL	Provides continuous control of the data output upper level from approximately -4 V to +5 V into 50 ohms (-8 V to +10 V open circuit).
2.9.2 LOWER LEVEL	Provides continuous control of the data output lower level from approximately -5 V to +4 V into 50 ohms (-10 V to +8 V open circuit).
2.10 EXTERNAL INPUTS	
2.10.1 CLOCK	Input connector for an external clock source. A 0 to +2 V pulse is required for trigger.
2.10.2 SYNC GATE	Input connector for a sync gate signal. A +2 V pulse is required for gating. The output occurs only during the time that the signal is applied.
2.10.3 RECYCLE	Input connector for a recycle command signal. A +2 V signal is required for recycling. A 16-bit word is generated for each recycle command signal.

2.11 SYNC OUTPUTS

2.11.1 CLOCK — Output connector for the clock sync. This sync output occurs at the data rate.

2.11.2 BIT 1 — Output connector for Bit 1 sync. This sync output occurs approximately 20 ns before the first bit in each data cycle (16-bit word).

2.11.3 BIT 16 — Output connector for Bit 16 sync. This sync output occurs approximately 20 ns before the last bit in each data cycle (16-bit word).

2.12 OUTPUT

2.12.1 TRUE — Output connector for positive true data. The amplitude and baseline are variable by means of the UPPER and LOWER level controls.

2.12.2 COMPLEMENT — Output connector for data that is the complement of the data at the TRUE output.

2.13 115/230 V Selector (Back Panel) — Selects the transformer primary configuration for either 115 or 230 V ac.

CHAPTER 3
OPERATION

3.1 FUNCTIONAL VERIFICATION

The following procedure provides a brief operational check of the instrument and an introduction to its controls.

3.1.1 Equipment (or equivalent) Required

a. A pulse source capable of 50 MHz repetition rate and +2 V amplitude. Systron-Donner Model 110B Pulse Generator recommended.

b. A dual-trace real-time oscilloscope with a 50 MHz bandwidth. Tektronix 546 with a Type 1A2 plug-in recommended.

c. Two 50 ohm, 2 watt terminations. Tektronix 011-0049-01.

d. Four 50 ohm coaxial cables (2-3 feet long) terminated with BNC connectors.

3.1.2 Data Output Verification

a. Set the instrument controls as follows:

Control	Setting
CLOCK RATE	10 kHz
CLOCK RATE vernier	fully clockwise
WIDTH	100 µs
WIDTH vernier	mid-range
DATA CONTENT	odd numbers depressed
FORMAT	NRZ depressed
RECYCLE	CONT depressed
UPPER LEVEL	+5
LOWER LEVEL	0
SYNC GATE	off
BIT 16	RZ

b. Monitor the TRUE and COMPLEMENT OUTPUTS on the dual-trace real-time oscilloscope. Trigger the oscilloscope from the BIT 1 SYNC OUTPUT. Terminate all three outputs with the 50 ohm, 2 watt terminations.

c. Set the oscilloscope controls to display one data cycle (16-bit word).

d. Verify that the odd numbered bits are true (+5 V logic level) for the entire bit period (approximately 100 µs) and the even numbered bits are false (0 V logic level) at the TRUE OUTPUT. Verify that the bits at the COMPLEMENT OUTPUT are the inverse of the bits at the TRUE OUTPUT.

e. Release the odd numbered DATA CONTENT pushbuttons and depress the even numbered pushbuttons. Verify that the even numbered bits are true (+5 V logic level) and the odd numbered bits are false (0 V logic level) at the TRUE OUTPUT. Verify that the bits at the COMPLEMENT OUTPUT are the inverse of the bits at

the TRUE OUTPUT. Verify that bit 16 returns to the lower logic level one bit period after it begins.

f. Using the OUTPUT LEVEL controls verify that the upper logic level of the data can be varied from approximately -4 V to +5 V and the lower logic level can be varried from approximately -5 V to + 4 V.

NOTE: Maximum difference between the upper and lower logic levels should be slightly greater than 5 volts.

g. Set the UPPER LEVEL control to +5 V and the LOWER LEVEL control to 0 V.

h. Depress the 50 MHz CLOCK RATE pushbutton and set the CLOCK RATE vernier fully clockwise. Verify that the clock rate is greater than 50 MHz. Set the CLOCK RATE vernier fully counterclockwise and verify that the clock rate is less than 10 MHz.

i. Check the remaining CLOCK RATE ranges and verify overlap at the upper and lower limits.

j. Depress the 10 kHz CLOCK RATE pushbutton and set the CLOCK RATE vernier fully clockwise.

k. Depress the RZ (FORMAT) pushbutton and verify that the bits are true (+5 V logic level) for approximately 50% of the bit period.

l. Rotate the WIDTH vernier counterclockwise and verify that the bit width decreases. Rotate the WIDTH vernier clockwise and verify that the bit width increases. Set the WIDTH vernier counterclockwise.

m. Sync scope on CLOCK SYNC output. Depress the PULSE (FORMAT) pushbutton and verify that the output changes from a data to a pulse format (pulse occurs approximately ever 100 µs).

n. Depress the NRZ (FORMAT) and the SYNC (RECYCLE COMMAND) pushbutton. Connect the external pulse generator to the RECYCLE INPUT. Set the external pulse generator for 100 Hz repetition rate, 20 ns width and +2 V amplitude (0 V baseline). Trigger the oscilloscope from the sync output of the external generator.

o. Verify that a 16-bit word is generated approximately every 10 ms. Verify that the 16th bit returns to zero 1 bit period after it begins. Set the BIT 16 switch to NRZ and verify that bit 16 remains true until the beginning of the first bit of the next data cycle.

p. Depress the ASYNC (RECYCLE COMMAND) pushbutton and verify that 16-bit words are generated at approximately a 10 ms rate.

NOTE: Only the first cycle of data output will be stable since the clock is not synchronized to the recycle input signal.

q. Disconnect the external pulse generator from the RECYCLE INPUT. Depress the MAN (RECYCLE COMMAND) pushbutton and verify that a 16-bit word is generated each time the pushbutton is depressed.

3.1.3 Sync Gate Verification

a. Set the instrument controls the same as in paragraph 3.1.2, step (a).

b. Connect the external pulse generator to the SYNC GATE INPUT. Set the pulse generator for 1 kHz repetition rate, +2 V amplitude (0 V baseline) and 500 µs pulse width.

c. Monitor the TRUE OUTPUT with the real-time oscilloscope. Trigger the oscilloscope from the sync output of the external pulse generator.

d. Set the SYNC GATE switch to ON.

e. Depress the PULSE (FORMAT) pushbutton and verify that the pulse output is gated.

3.1.4 Sync Output Verification

a. Set the instrument controls the same as in paragraph 3.1.2, step (a).

b. Monitor the TRUE and BIT 1 SYNC OUTPUTS on the dual-trace oscilloscope. Trigger the oscilloscope from the BIT 16 SYNC OUTPUT. Terminate all three outputs with the 50 ohm, 2 watt terminations at the oscilloscope.

c. Verify that BIT 1 SYNC OUTPUT has an amplitude of >+2 V and occurs approximately 30 ns before the first bit of the data output.

d. Disconnect the BIT 1 SYNC OUTPUT from the oscilloscope and monitor the BIT 16 SYNC OUTPUT. Verify that the BIT 16 SYNC OUTPUT has an amplitude of >+2 V and occurs approximately 30 ns before the sixteenth bit of the data output.

e. Disconnect the BIT 16 SYNC OUTPUT and monitor the CLOCK SYNC OUTPUT. Verify that the CLOCK SYNC OUTPUT has an amplitude of >+2 V and occurs at the data rate.

3.1.5 External and Manual Trigger Verification

a. Connect the external pulse generator to the CLOCK input. Set the pulse generator for a repetition rate of 10 kHz, and amplitude of +2 V (0 V baseline) and 20 ns width.

b. Monitor the TRUE OUTPUT on the real-time oscilloscope. Trigger the oscilloscope from the BIT 1 SYNC OUTPUT of the external pulse generator. Terminate both outputs with the 50 ohm, 2 watt terminations.

c. Set the instrument controls the same as in paragraph 3.1.2, step (a) except depress the EXT (CLOCK RATE) pushbutton.

d. Verify that the instrument is triggered (data output occurs with a format corresponding to the position of the DATA CONTENT pushbuttons).

e. Verify that the instrument can be triggered from 10 Hz to 50 MHz.

f. Disconnect the external pulse generator. Trigger the oscilloscope from the BIT 1 SYNC OUTPUT.

g. Depress the MAN (CLOCK RATE) pushbutton sixteen times and verify that a TRUE OUTPUT occurs.

CHAPTER 4
CALIBRATION

4.1 EQUIPMENT (or equivalent) REQUIRED

a. A real-time oscilloscope with a bandwidth of 50 MHz. Tektronix Type 546 with a 1A2 plug-in recommended.

b. A sampling oscilloscope with a 0.35 ns rise time. Tektronix Type 546 with a 1S1 plug-in recommended.

c. An electronic counter with a 50 MHz capability. Systron-Donner Model 6150 recommended.

d. A pulse source capable of 50 MHz repetition rate and >+2 V amplitude. Systron-Donner Model 110B recommended.

e. A digital voltmeter capable of reading millivolts. Systron-Donner Model 700A recommended.

f. Two 50 ohm, 2 watt coaxial terminations. Systron-Donner Type 2010 recommended.

g. Two 10X, 2 watt, 50 ohm attenuators. Tektronix 011-0059-01 recommended.

h. Several 50 ohm coaxial cables terminated with BNC connectors.

4.2 POWER SUPPLY CALIBRATION

a. Connect the instrument to the 115 V supply and set the POWER switch to ON. Depress the EXT (CLOCK RATE) pushbutton.

b. Monitor the +15 V buss with the digital voltmeter and adjust R529 for +15.00 volts.

c. Monitor the -15 V buss with the digital voltmeter and verify a reading of -15.00 ±0.3 V.

d. Monitor the +5 V buss with the digital voltmeter and verify a reading of +5.00 ±0.1 V.

4.3 CLOCK RATE CALIBRATION

a. Set the instrument controls as follows:

Control	Setting
CLOCK RATE	50 MHz
CLOCK RATE vernier	fully counterclockwise
FORMAT	PULSE
WIDTH	100 ns
WIDTH vernier	fully counterclockwise
UPPER LEVEL	+5 V
LOWER LEVEL	0 V

b. Monitor the TRUE OUTPUT on the counter. Terminate the output with the 50 ohm, 2 watt termination at the counter input.

c. Adjust C31 for a counter indication of approximately 9.5 MHz.

d. Set the CLOCK RATE vernier fully clockwise and verify that the clock rate is >50 MHz.

e. Check the remaining clock rate ranges for overlap at the upper and lower limits.

NOTE: Check the appropriate timing capacitors (C21 through C26) if it is not possible to get overlap on all ranges.

4.4 CLOCK WIDTH CALIBRATION

a. Set the instrument controls the same as in paragraph 4.3, step (a) except select the 10 MHz clock rate range.

b. Monitor TP1K with the sampling oscilloscope. Trigger the oscilloscope from the CLOCK SYNC OUTPUT. Adjust C82 for a clock pulse width of 8 ns.

4.5 BIT 16 RZ CALIBRATION

a. Set the instrument controls as follows:

Control	Setting
CLOCK RATE	50 MHz
CLOCK RATE vernier	fully clockwise
FORMAT	RZ
WIDTH	100 ns
WIDTH vernier	fully counterclockwise
BIT 16	RZ
RECYCLE COMMAND	SYNC
UPPER LEVEL	+5 V
LOWER LEVEL	0 V

b. Connect the external pulse source to the RECYCLE INPUT. Set the source for a repetition rate of 1 MHz and an amplitude of +2 V.

c. Monitor the TRUE OUTPUT with the sampling oscilloscope. Trigger the oscilloscope from the BIT 1 SYNC OUTPUT.

d. Depress all DATA CONTENT pushbuttons except number 15. Adjust C173 so that Bit 16 is true for the same period of time that Bit 16 is false.

4.6 WIDTH/RZ CALIBRATION

a. Set the instrument controls as follows:

Control	Setting
CLOCK RATE	1 MHz
CLOCK RATE vernier	mid-range
FORMAT	PULSE
WIDTH	100 ns
WIDTH vernier	fully clockwise
UPPER LEVEL	+5 V
LOWER LEVEL	0 V

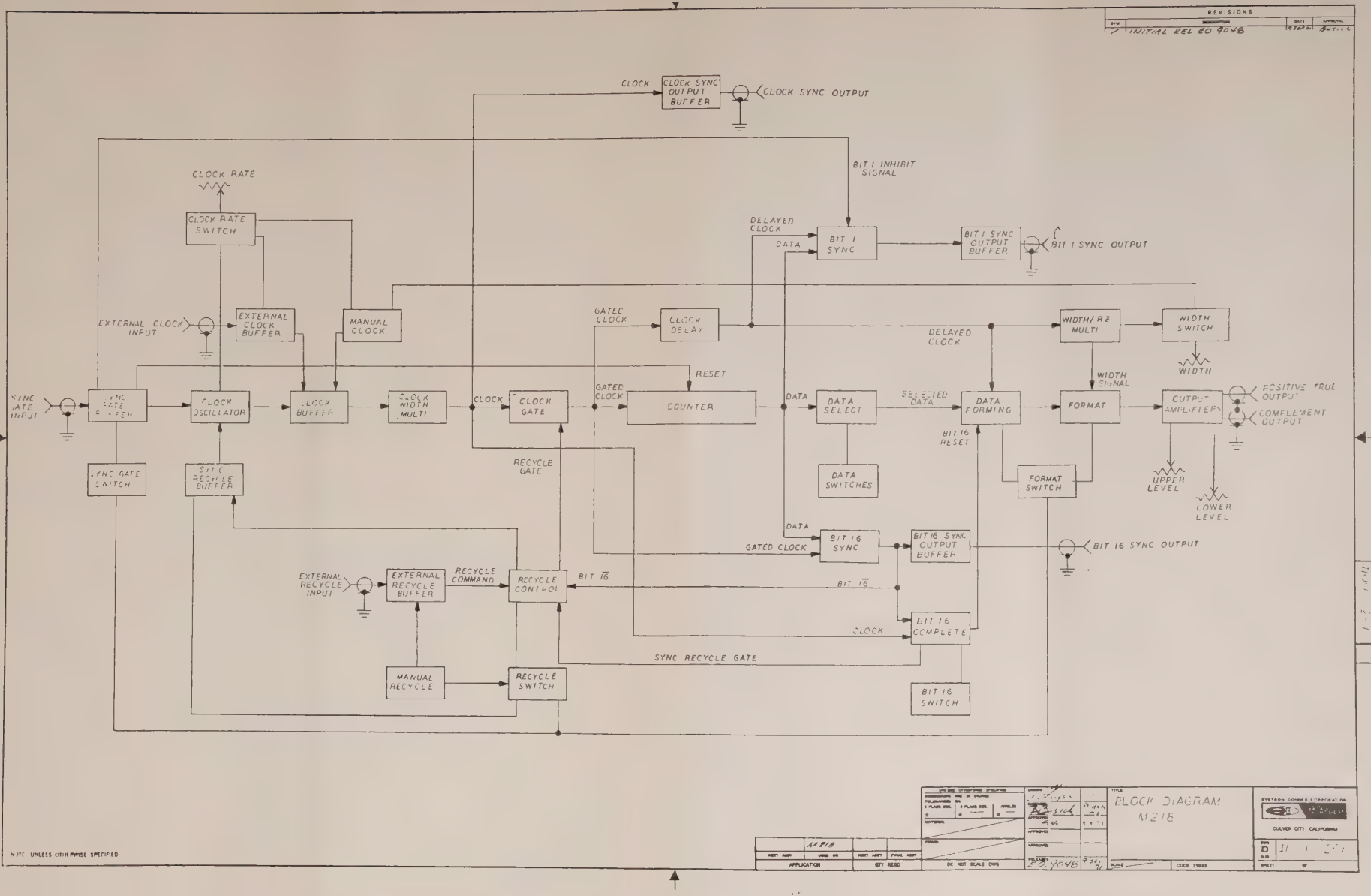
b. Monitor the TURE OUTPUT with the sampling oscilloscope. Trigger the oscilloscope from the CLOCK SYNC OUTPUT. Terminate both outputs with the 50 ohm, 10X attenuators.

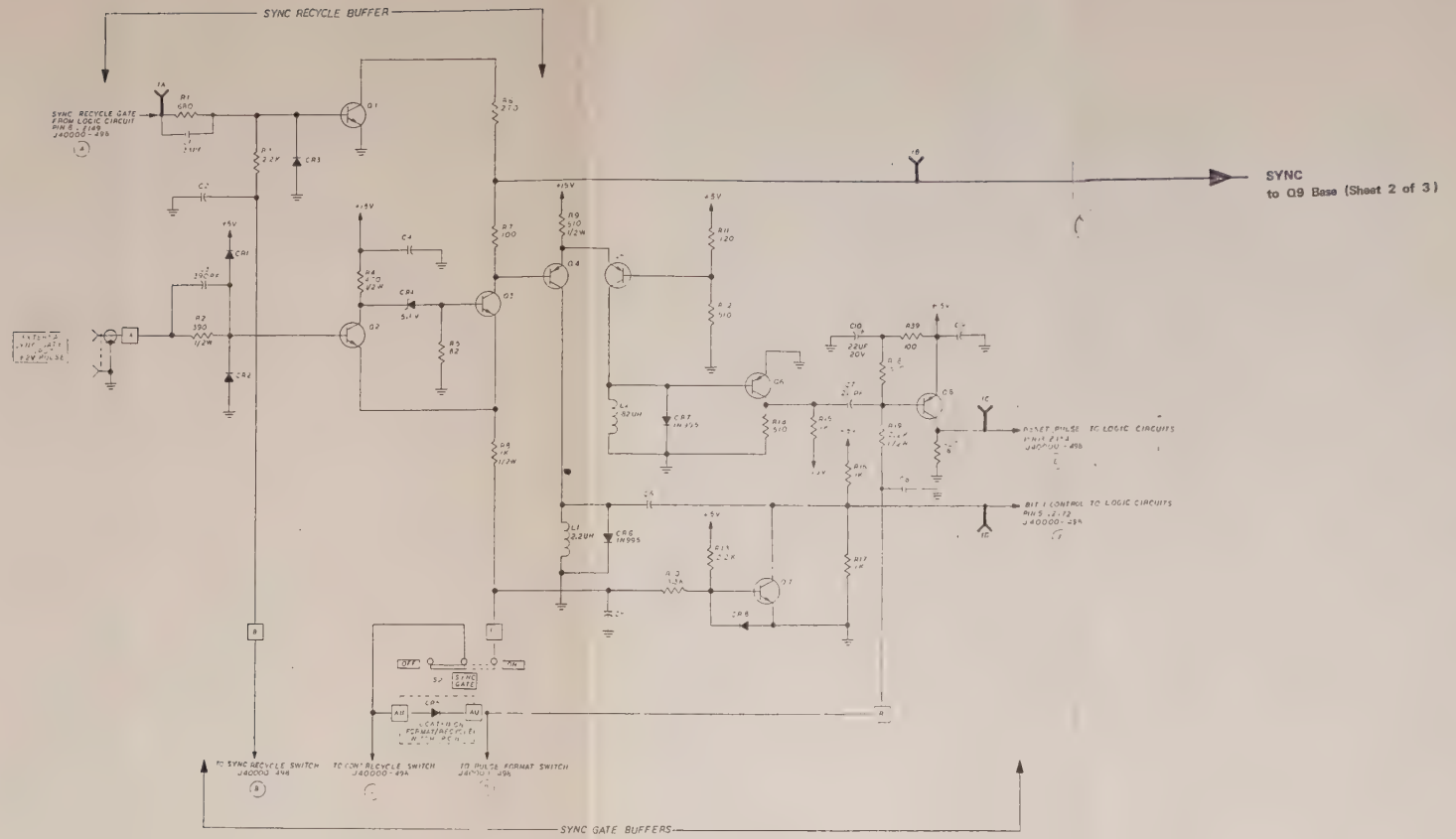
c. Adjust C218 for a pulse width of approximately 110 ns.

d. Set the pulse width vernier fully counterclockwise and verify a pulse width of approximately 10 ns or less.

e. Check the remaining width ranges for overlap at the upper and lower limit. Use the real-time oscilloscope to check all but the 1 µs and 100 ns ranges. Attenuate the OUTPUT and SYNC OUTPUT with the 50 ohm, 10X attenuator when using the sampling oscilloscope.

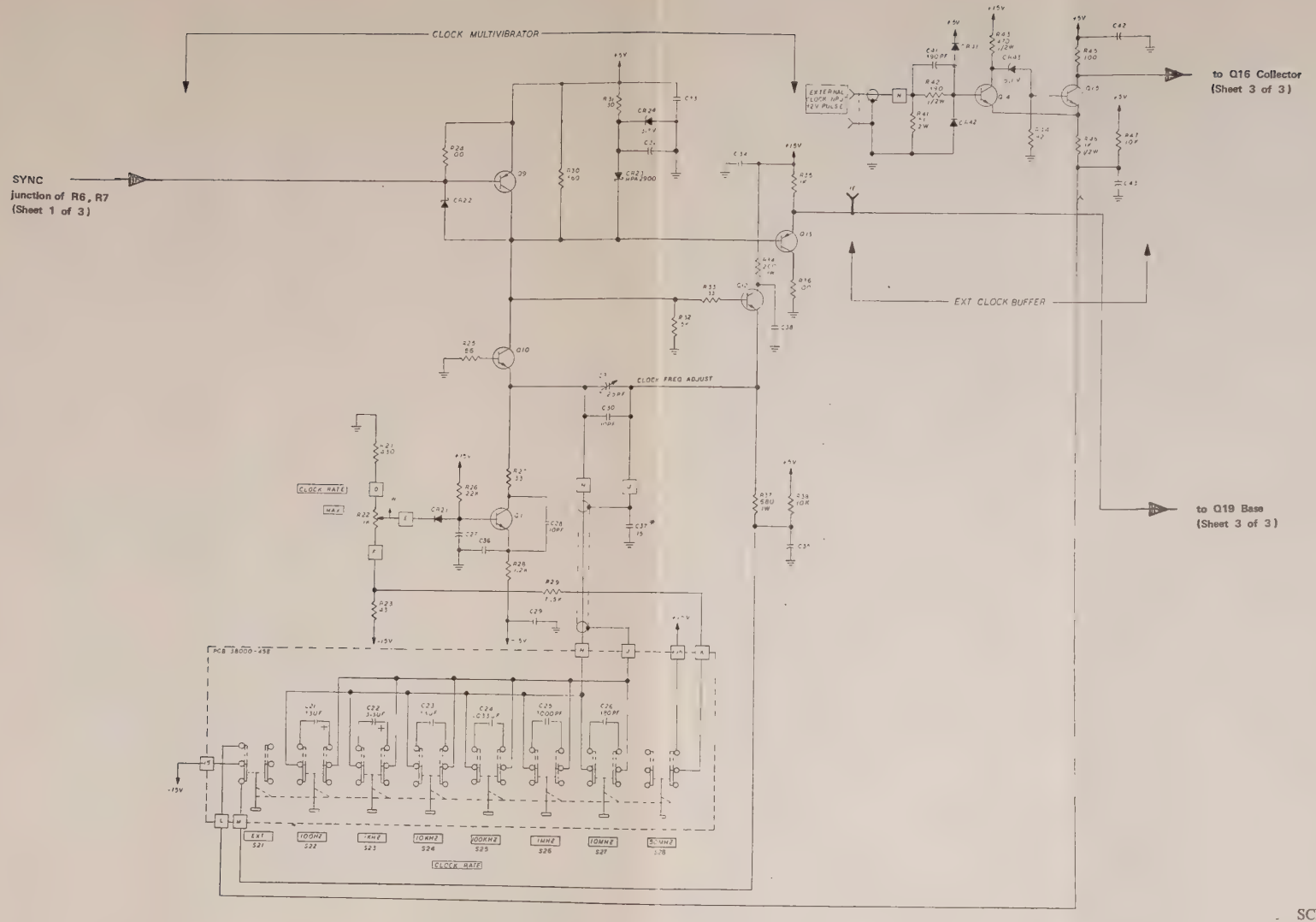
NOTE: If it is not possible to get overlap on all ranges, check the appropriate timing capacitor (C250 through C254).


REVISIONS
INITIAL REL TO 9048
CLOCK
CLOCK SYNC OUTPUT BUFFER
CLOCK SYNC OUTPUT
BIT 1 INHIBIT SIGNAL
CLOCK RATE
CLOCK RATE SWITCH
DELAYED CLOCK
DATA
BIT 1 SYNC
BIT 1 SYNC OUTPUT BUFFER
BIT 1 SYNC OUTPUT
EXTERNAL CLOCK INPUT
EXTERNAL CLOCK BUFFER
MANUAL CLOCK
GATED CLOCK
CLOCK DELAY
DELAYED CLOCK
WIDTH/RZ MULTI
WIDTH SWITCH
WIDTH
RESET
WIDTH SIGNAL
SYNC GATE INPUT
SYNC GATE BUFFER
CLOCK OSCILLATOR
CLOCK BUFFER
CLOCK WIDTH MULTI
CLOCK
CLOCK GATE
GATED CLOCK
COUNTER
DATA
DATA SELECT
SELECTED DATA
DATA FORMING
FORMAT
OUTPUT AMPLIFIER
POSITIVE TRUE OUTPUT
COMPLEMENT OUTPUT
BIT 16 RESET
SYNC GATE SWITCH
BIT RECYCLE BUFFER
RECYCLE GATE
DATA SWITCHES
FORMAT SWITCH
UPPER LEVEL
LOWER LEVEL
DATA
BIT 16 SYNC
BIT 16 SYNC OUTPUT BUFFER
GATED CLOCK
BIT 16 SYNC OUTPUT
EXTERNAL RECYCLE INPUT
EXTERNAL RECYCLE BUFFER
RECYCLE COMMAND
RECYCLE CONTROL
BIT 16
BIT 16
BIT 16 COMPLETE
CLOCK
SYNC RECYCLE GATE
MANUAL RECYCLE
RECYCLE SWITCH
BIT 16 SWITCH
NOTE UNLESS OTHERWISE SPECIFIED
APPLICATION
CITY REED
DO NOT SCALE DWG
BLOCK DIAGRAM
M218
SCALE
CODE 19843
SIZE D
SHEET

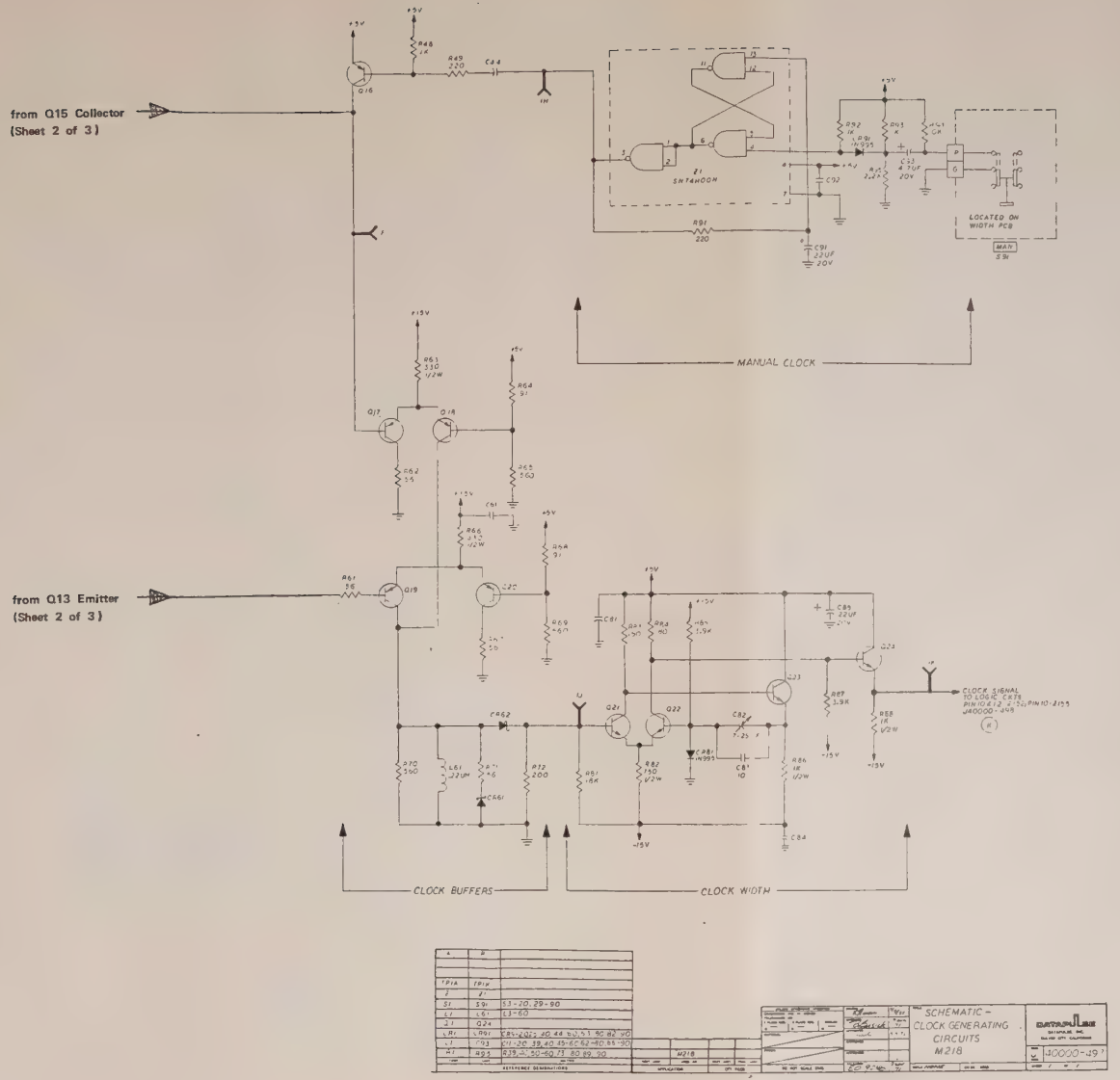


9. * INDICATES A FACTORY SELECTED VALUE SUBJECT TO CHANGE & MAY OR MAY NOT BE PRESENT.
8. ⊠ INDICATES HOT CARRIER DIODE HPA5082-2811.
7. CIRCLED LETTERS ARE FOR REFERENCE.
6. BOXED LETTERS INDICATE SPECIFIC LABELED POINTS ON PCB.
5. BOXED WORDING INDICATES FRONT PANEL NOMENCLATURE.
4. ALL NPN TRANSISTORS ARE DP653/2N2369A ALL PNP ARE EP60B.
3. ALL DIODES ARE DP16-01/IN3600.
2. ALL CAPACITORS ARE .022 UF 25V.
1. ALL RESISTORS ARE IN OHMS 1/4W 5%.
NOTE: UNLESS OTHERWISE SPECIFIED

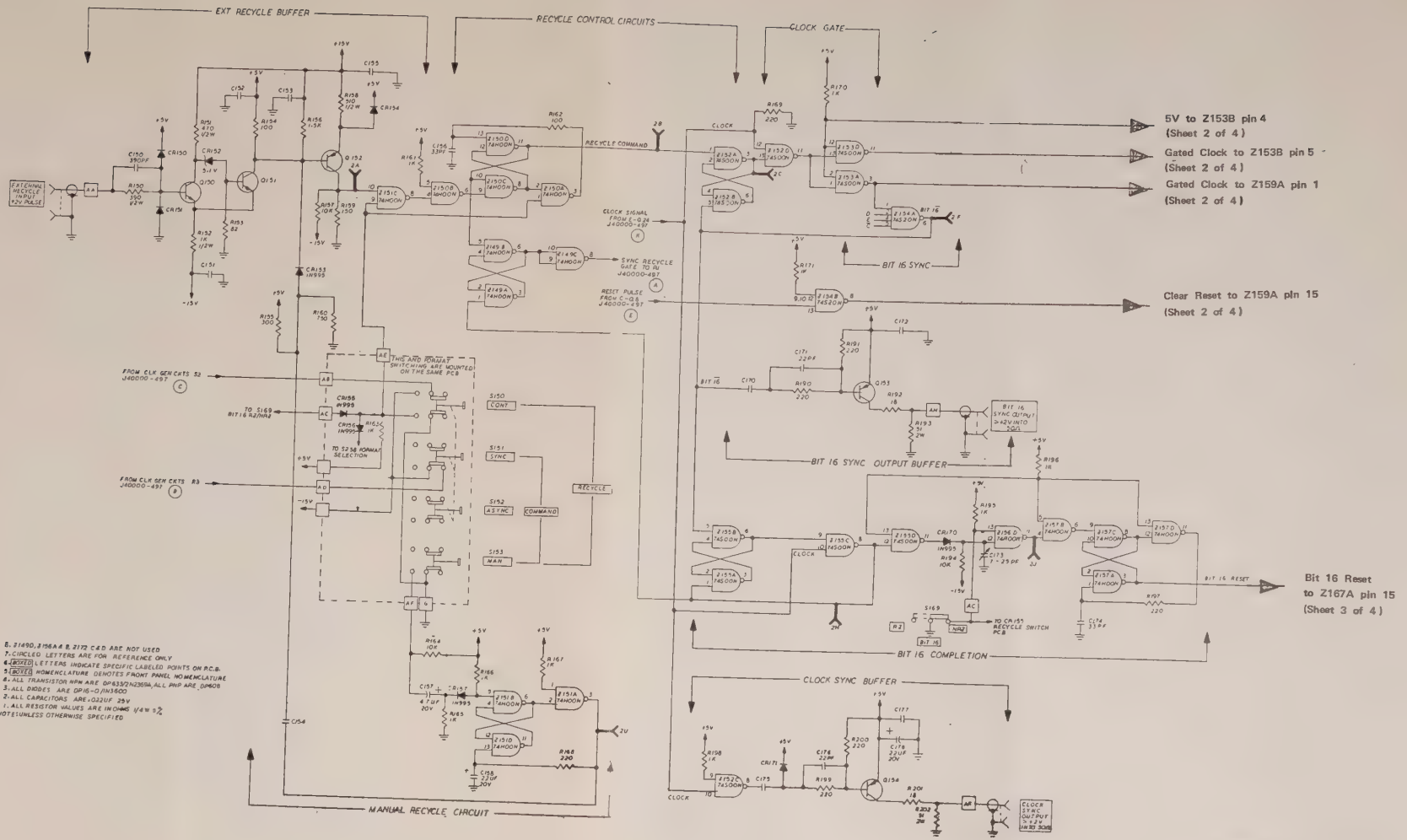
SCHEMATIC , 40000-497
CLOCK GENERATING
CIRCUITS M218



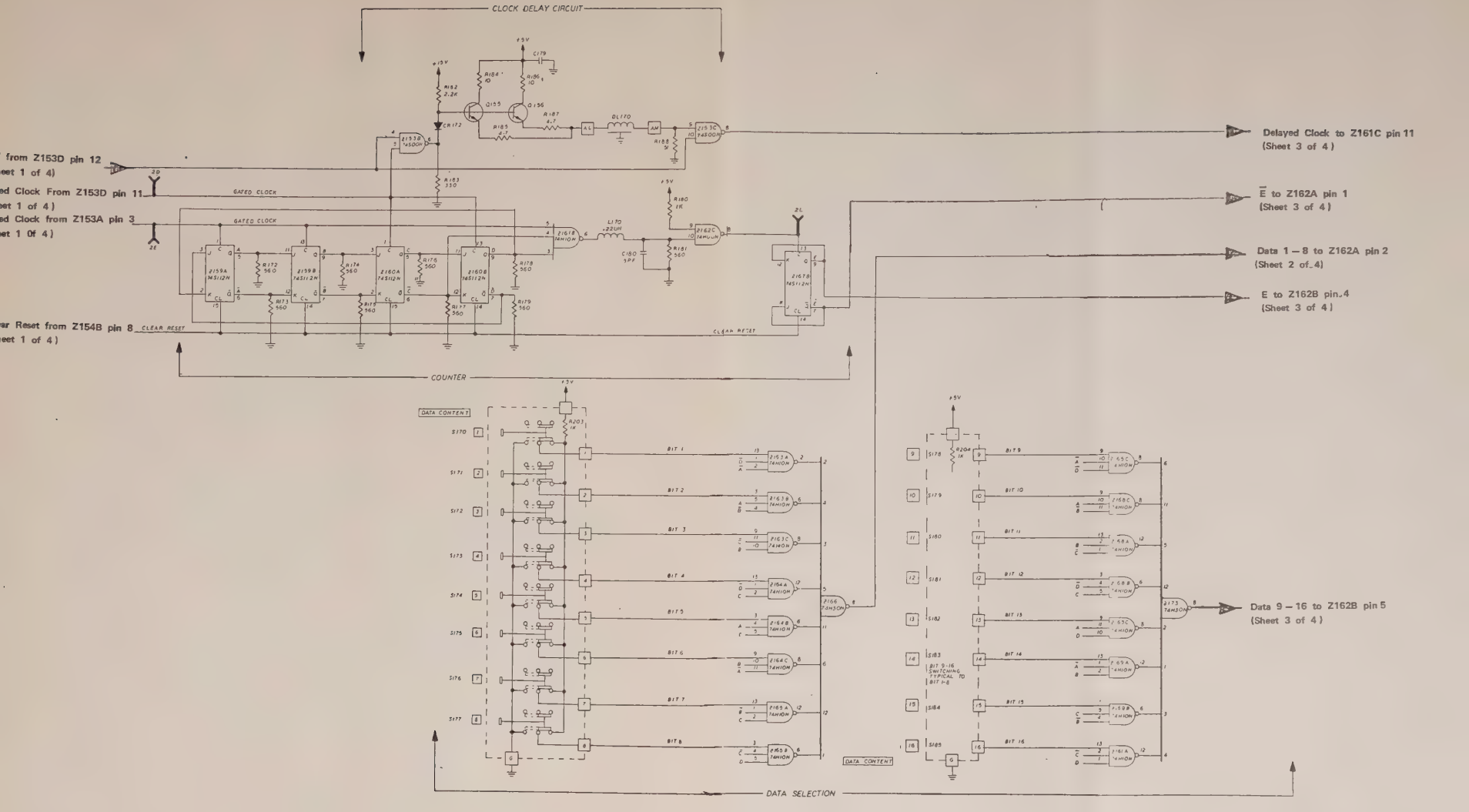
SCHEMATIC, 40000-497
CLOCK GENERATING
CIRCUITS M218



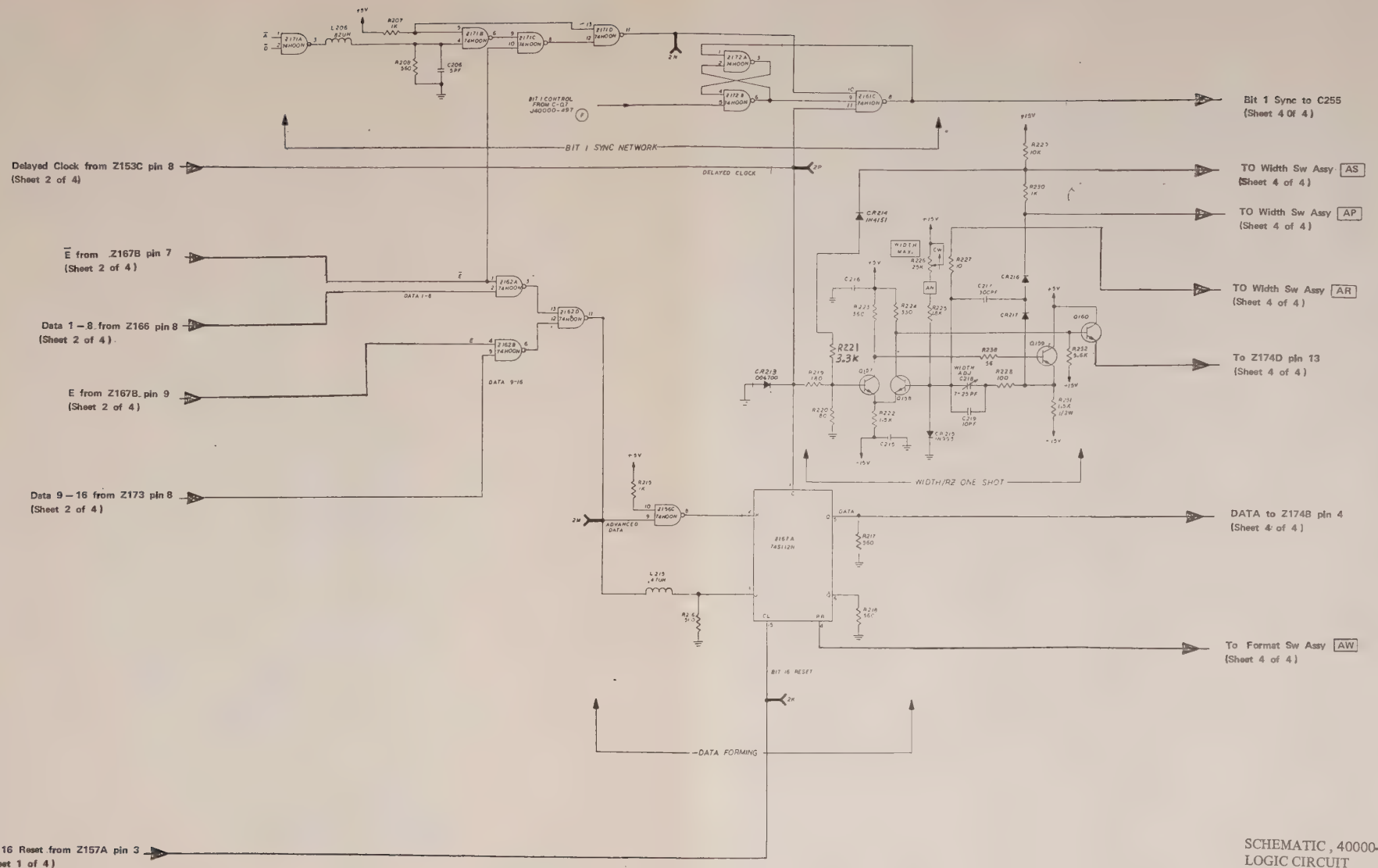
SCHEMATIC , 40000-497
CLOCK GENERATING
CIRCUITS M218
PAGE 3 OF 3 PAGES


EXT RECYCLE BUFFER
RECYCLE CONTROL CIRCUITS
CLOCK GATE
5V to Z153B pin 4 (Sheet 2 of 4)
Gated Clock to Z153B pin 5 (Sheet 2 of 4)
Gated Clock to Z159A pin 1 (Sheet 2 of 4)
Clear Reset to Z159A pin 15 (Sheet 2 of 4)
Bit 16 Reset to Z167A pin 15 (Sheet 3 of 4)
RECYCLE COMMAND
CLOCK SIGNAL FROM E-0.24 J40000-497
SYNC RECYCLE GATE TO AJ J40000-497
RESET PULSE FROM C-0.8 J40000-497
BIT 16 SYNC
BIT 16 SYNC OUTPUT BUFFER
BIT 16 COMPLETION
CLOCK SYNC BUFFER
MANUAL RECYCLE CIRCUIT
FROM CLK GEN CKTS S3 J40000-497
FROM CLK GEN CKTS R3 J40000-491
TO S169 BIT 16 RQ/INAQ
TO S2 16 FORMAT SELECTION
THESE CARD FORMAT SWITCHING ARE MOUNTED ON THE SAME PCB
S150 CONT
S151 SYNC
S152 ASYNC
S153 MAN
RECYCLE
COMMAND
TO CA151 RECYCLE SWITCH PCB
8. Z1490, Z1564 & Z172 C&D ARE NOT USED
7. CIRCLED LETTERS ARE FOR REFERENCE ONLY
6. BOXED LETTERS INDICATE SPECIFIC LABELED POINTS ON P.C.B.
5. BOXED NOMENCLATURE DENOTES FRONT PANEL NOMENCLATURE
4. ALL TRANSISTOR NPN ARE DP6332/N2369A, ALL PNP ARE DM608
3. ALL DIODES ARE DP15-0/1N3600
2. ALL CAPACITORS ARE +.022UF 25V
1. ALL RESISTOR VALUES ARE IN OHMS 1/4W ±5%
NOTE: UNLESS OTHERWISE SPECIFIED

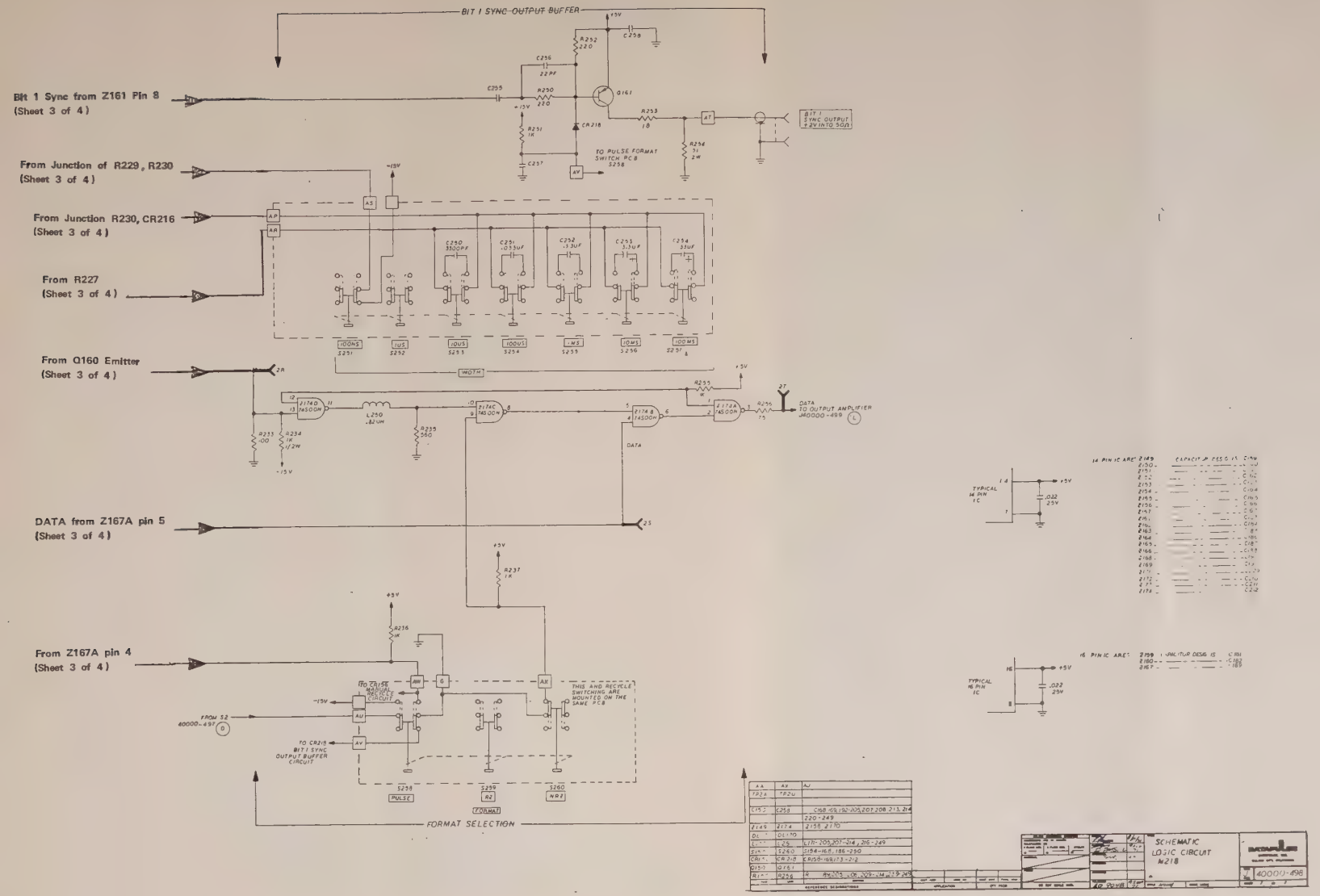
SCHEMATIC, 40000-498
LOGIC CIRCUIT
M218


CLOCK DELAY CIRCUIT
from Z153D pin 12 (Sheet 1 of 4)
ed Clock From Z153D pin 11 (Sheet 1 of 4)
ed Clock from Z153A pin 3 (Sheet 1 Of 4)
er Reset from Z154B pin 8 (Sheet 1 of 4)
GATED CLOCK
CLEAR RESET
COUNTER
Delayed Clock to Z161C pin 11 (Sheet 3 of 4)
E to Z162A pin 1 (Sheet 3 of 4)
Data 1 – 8 to Z162A pin 2 (Sheet 2 of 4)
E to Z162B pin 4 (Sheet 3 of 4)
DATA CONTENT
DATA SELECTION
Data 9 – 16 to Z162B pin 5 (Sheet 3 of 4)

SCHEMATIC , 40000-498
LOGIC CIRCUIT
M218
PAGE 2 OF 4 PAGES

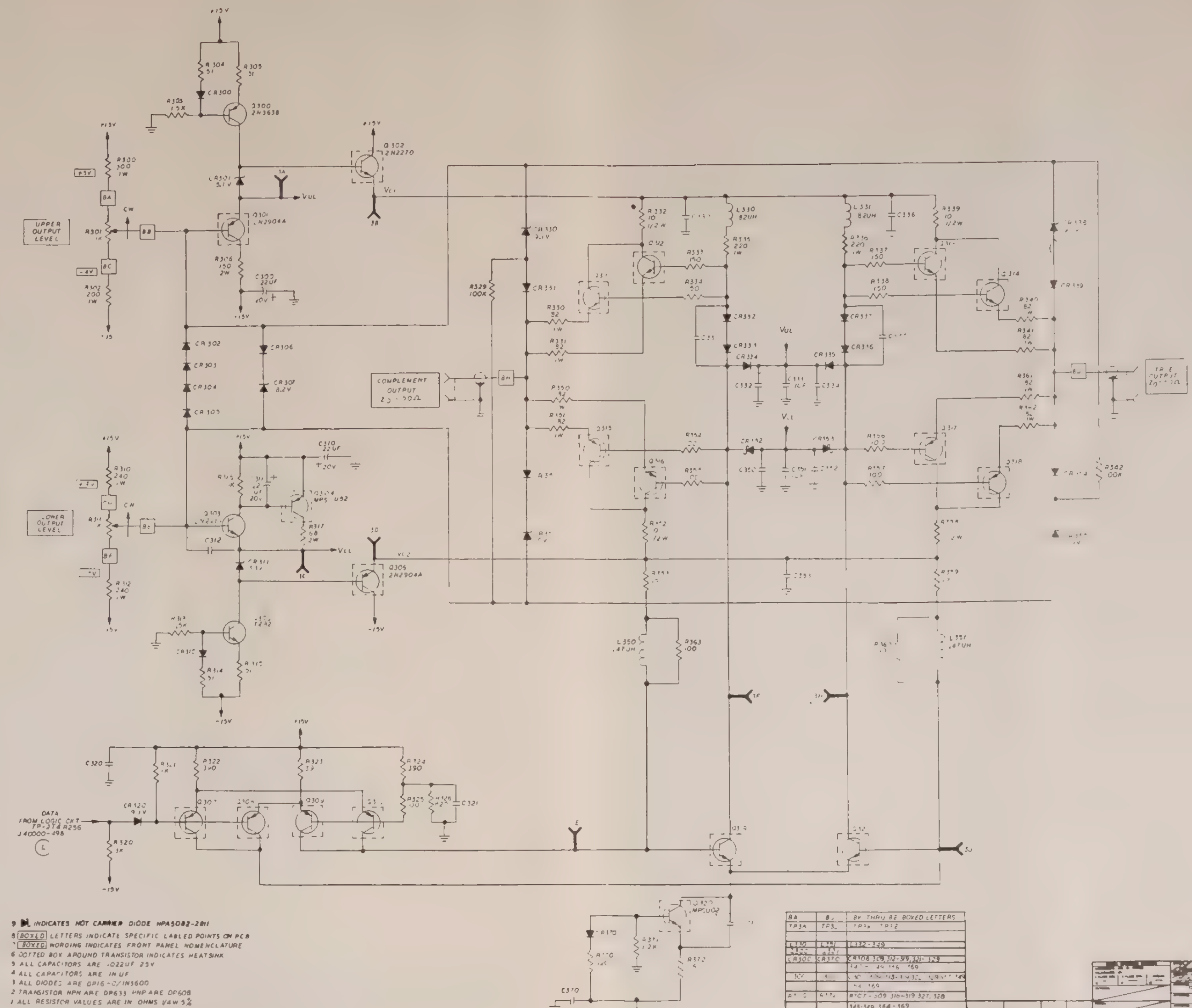

Bit 1 Sync to C255
(Sheet 4 Of 4)
BIT 1 SYNC NETWORK
Delayed Clock from Z153C pin 8
(Sheet 2 of 4)
DELAYED CLOCK
TO Width Sw Assy AS
(Sheet 4 of 4)
TO Width Sw Assy AP
(Sheet 4 of 4)
Ē from Z167B pin 7
(Sheet 2 of 4)
TO Width Sw Assy AR
(Sheet 4 of 4)
Data 1 – 8 from Z166 pin 8
(Sheet 2 of 4)
To Z174D pin 13
(Sheet 4 of 4)
E from Z167B pin 9
(Sheet 2 of 4)
Data 9 – 16 from Z173 pin 8
(Sheet 2 of 4)
WIDTH/RZ ONE SHOT
DATA to Z174B pin 4
(Sheet 4 of 4)
To Format Sw Assy AW
(Sheet 4 of 4)
BIT 16 RESET
DATA FORMING
Bit 16 Reset from Z157A pin 3
(Sheet 1 of 4)

SCHEMATIC , 40000-498
LOGIC CIRCUIT
M218


BIT 1 SYNC OUTPUT BUFFER
Bit 1 Sync from Z161 Pin 8
(Sheet 3 of 4)
From Junction of R229, R230
(Sheet 3 of 4)
From Junction R230, CR216
(Sheet 3 of 4)
From R227
(Sheet 3 of 4)
From Q160 Emitter
(Sheet 3 of 4)
DATA from Z167A pin 5
(Sheet 3 of 4)
From Z167A pin 4
(Sheet 3 of 4)
BIT 1 SYNC OUTPUT + 2V INTO 50Ω
TO PULSE FORMAT SWITCH PCB 5258
DATA TO OUTPUT AMPLIFIER J40000-499
TO CR216 BIT 1 SYNC OUTPUT BUFFER CIRCUIT
FROM 52 40000-497
THIS AND RECYCLE SWITCHING ARE MOUNTED ON THE SAME PCB
PULSE
FORMAT
FORMAT SELECTION
TYPICAL 14 PIN IC
TYPICAL 16 PIN IC
SCHEMATIC LOGIC CIRCUIT M218
40000-498

SCHEMATIC , 40000-498
LOGIC CIRCUIT
M218
PAGE 4 OF 4 PAGES

		REVISIONS		
		INITIAL REL EO [illegible]		
	A	INCORP EO [illegible]		
	B	INCORP E.O. 8307		



+15V
R304 51
R305 51
CR300
R303 1.5K
Q300 2N3638
R300 300 1W
+5V
BA
UPPER OUTPUT LEVEL
R301 1K
CW
BB
BC
-4V
R302 200 1W
CR301 5.1V
1A
VUL
Q301 2N2904A
R306 150 2W
C300 22UF 20V
-15V
Q302 2N2270
VCI
3B
CR302
CR303
CR304
CR305
CR306
CR307 8.2V
R310 240 1W
LOWER OUTPUT LEVEL
C310 22UF 20V
Q304 MPS U52
R317 68 2W
C312
VLL
3C
3D
Q305 2N2904A
R312 240 1W
R315 51
R314 51
-15V
CR330 9.1V
CR331
R329 100K
R330 82 1W
R331 82 1W
COMPLEMENT OUTPUT 25 - 50Ω
BH
R350 82
R351 82 1W
R332 10 1/2W
L330 82UH
R335 220 1W
R333 150
R334 50
CR332
CR333
CR334
CR335
C332
C334
VUL
L331 82UH
C336
R336 220 1W
R337 150
R338 150
R339 10 1/2W
CR336
R340 82
R341 82 1A
CR338
CR339
BJ
R361 82 1W
R342 100K
Q316
Q318
R357 100
R363 100
L350 .47UH
L351 .47UH
3F
3J
E
C320
R322 390
R321 33
R324 390
R325 100
C321
CR320 9.1V
DATA FROM LOGIC CKT TP-2T & R256 J 40000-498
R320 3K
-15V
Q370 MPSU02
CR370
R370 12K
R371 12K
R372
C370

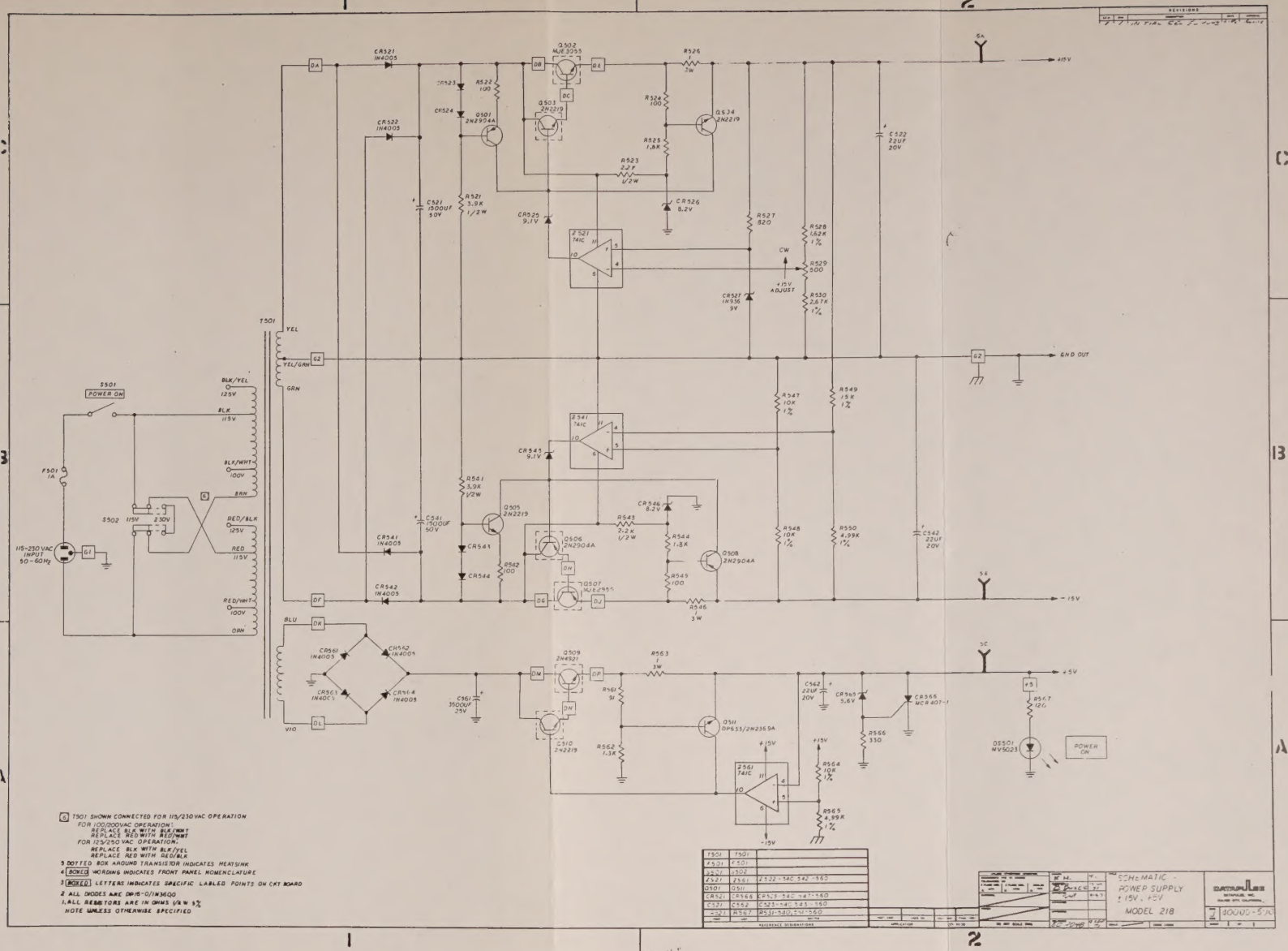
9 [diode symbol] INDICATES HOT CARRIER DIODE HPA5082-2811
8 [BOXED] LETTERS INDICATE SPECIFIC LABLED POINTS ON PCB
7 [BOXED] WORDING INDICATES FRONT PANEL NOMENCLATURE
6 DOTTED BOX AROUND TRANSISTOR INDICATES HEATSINK
5 ALL CAPACITORS ARE .022UF 25V
4 ALL CAPACITORS ARE IN UF
3 ALL DIODES ARE DP16-C/IN3600
2 TRANSISTOR NPN ARE DP633 PNP ARE DP608
1 ALL RESISTOR VALUES ARE IN OHMS 1/4W 5%
NOTE UNLESS OTHERWISE SPECIFIED

BA	BJ	BK THRU BZ BOXED LETTERS
TP3A	TP3_	TP3K TP3Z
L350	L351	L332-349
CA30C	CR370	CR308 309, 312-329, 321-329
		340 - 349 366 369
30V	[illegible]	[illegible]
		[illegible] 369
R300	R372	R307 - 309 310-319 327, 328
		343-349, 364-369
		REFERENCE DESIGNATIONS

SCHEMATIC - OUTPUT AMPLIFIER M216

40000-499

40000 499



G T501 SHOWN CONNECTED FOR 115/230 VAC OPERATION
FOR 100/200 VAC OPERATION:
REPLACE BLK WITH BLK/WHT
REPLACE RED WITH RED/WHT
FOR 125/250 VAC OPERATION:
REPLACE BLK WITH BLK/YEL
REPLACE RED WITH RED/BLK

3 DOTTED BOX AROUND TRANSISTOR INDICATES HEATSINK

4 BOXED WORDING INDICATES FRONT PANEL NOMENCLATURE

5 BOXED LETTERS INDICATES SPECIFIC LABLED POINTS ON CKT BOARD

2 ALL DIODES ARE 1N916 OR 1N3600

1. ALL RESISTORS ARE IN OHMS 1/4 W 5%
NOTE UNLESS OTHERWISE SPECIFIED

T501	T501
F501	F501
S501	S502
Z521	Z561
Q501	Q511
CR521	CR566
C521	C562
R521	R567

Z532-540, 542-565
CR523-540, 543-560
C523-540, 543-560
R531-540, 541-560

SCHEMATIC - POWER SUPPLY ±15V, +5V
MODEL 218

DATAPULSE
INCORPORATED
SAN DIEGO, CALIFORNIA

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